Sundance Multiprocessor Technology Limited **Design Specification**	Form : QCF51 Dated : 23 May 2001 Revision : 5.0 Approved : Mark Ainsworth

Unit / Module Name:	Quad DSP Module
Unit / Module Number:	SMT395Q
Used On:	
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Outline Description

The SMT395Q is Sundance's 4th generation of Texas Instruments 'C6x DSP TIM (Texas Instruments Module). This module uses 4 TMS320C6416T DSPs which have clock speeds of up to 1GHz.

The module also includes a Xilinx VirtexII-Pro (XC2VP70FF1704) FPGA which is configured to provide 'C4x style Comm-ports, a TIM compatible enhanced global bus, two Sundance High-Speed Busses (SHBs), 14 Sundance RSL, and other control functions.

The SMT395Q is, from the user's perspective, a multi-DSP version of the SMT395 Module, and an upgrade to the SMT361Q.

The SMT395Q is supported by the T.I. Code Composer Studio and 3L Diamond RTOS to enable full MultiDSP systems with minimum efforts by the programmers.

Approvals		Date
Managing Director		
Software Manager		
Design Engineer		

Revision History

	Changes Made	Issue	Initials
7/9/04	First draft based on 361Q.	1.0.0	GP
10/9/04	Added DSP bandwidth comment.	1.0.1	GP
10/9/04	Minor corrections/additions.	1.0.2	GP
16/9/04	Added DDR to block diagram.	1.0.3	GP
23/9/04	Power measurement section added.	1.0.4	GP
27/9/04	System control section added	1.0.5	GP
21/1/05	Updated pcb layout. Corrected flash size.	1.1.0	GP
10/3/05	Major update relating to MPS430 operation.	1.2.0	GP
1/4/05	Removed RS232 reference. Increased size of DSPA's SDRAM. Updated EMIF A&B clocks to show a single 120MHz source. Added jumper section.	1.3.0	GP
8/4/05	Added power consumption figure.	1.3.1	GP

Table of Contents

1 Introduction

1.1 Related Documents

General firmware user's guide. All details on the operation of the comm-ports, SDB/SHBs and global bus are in this document.

TIM Specification. Texas Instruments Module specification.

SHB Specification. Sundance High-speed Bus.

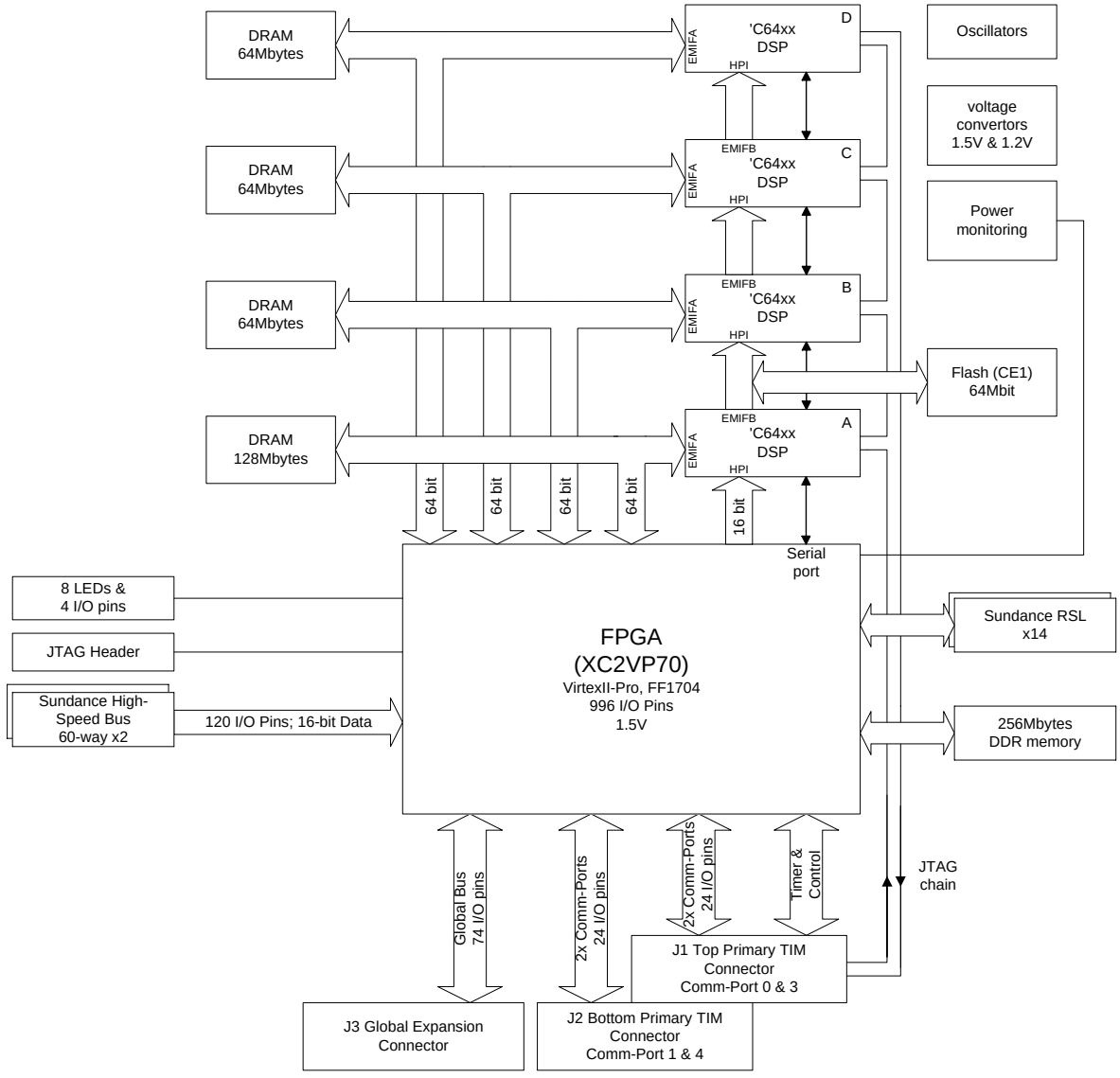
RSL Specification and Pin-out. Rocket IO Serial Link.

Diamond. Multi-DSP RTOS.

C6416T. TI DSP data sheet.

2 Functional Description

2.1 Block Diagram



2.2 Interface Description

2.2.1 Mechanical Interface

This module conforms to the TIM standard for double with modules. It requires an additional 3.3V power supply (as present on all Sundance TIM carrier boards) which must be provided by the four mounting holes.

2.2.2 Electrical Interface

2.2.2.1 Processor

The module is populated with four C6416T DSPs.

The following table shows the main DSP characteristics.

Feature	C6416T
DMA / McBSP / Timer	64/3/3
On-chip memory	1056k bytes
Speed	1GHz
Others	Viterbi and Turbo decoders

The JTAG interface is provided to enable application debugging via a suitable JTAG controller and software. Typically, this will be an SMT310Q and TI Code Composer Studio. This is an invaluable interface which enables the application programmer to quickly debug a 'chain' of processors in single or multi-processor situations.

The EMIFA is used to connect to the Virtex-II and SDRAM. EMIFB is use to connect to the adjacent DSP's Host Port Interface (HPI) and the Flash.

The flash memory is connected via EMIFB as a 16 bit device to DSP A only.

Memory space (EMIFA)	Resource	Address range
	Internal program memory (1M)	0x00000000 - 0x000FFFFF
CE0	SDRAM (64Mbytes)	0x80000000 - 0x83FFFFFF
CE1	SDRAM (64Mbytes) DSPA only	0x90000000 - 0x93FFFFFF
CE2	Virtex-II	0xA0000000 - 0xAFFFFFFF

The SDRAM in both CE spaces alias throughout that space. So, it is possible for DSPA to access its 128Mbyte SDRAM from address 0x8C000000 to 0x93FFFFFF.

Memory space (EMIFB)	Resource	Address range
CE0	HPI of adjacent DSP	0x60000000 - 0x600000FF
CE1	2Mbyte section of flash (DSP A only)	0x64000000 – 0x640FFFFF
CE2	FPGA PROG control (DSP A only). Write to this address to assert PROG and clear the FPGA configuration.	0x68000000
CE3	FPGA CCLK control (DSP A only)	0x6C000000

2.2.2.1.1 EMIFA Bus Bandwidth

The DSPs connect to the FPGA and SDRAMs using a 64 bit data bus. This operates synchronously at a speed of 120MHz.

The peak bus bandwidth is therefore 960 Mbytes/s.

2.2.2.1.2 DSP Heatsink

Each DSP is fitted with a AAVID Thermalloy heatsink (as per TI recommendation).

2.2.2.2 Flash

An 8Mbyte flash memory is provided with direct access by DSPA only. This device contains boot code for the DSP and the configuration data for the FPGA.

This is a 16-bit wide device.

As the DSP provides only 20 address pins, then the maximum addressable memory is 2Mbytes (16-bit EMIFB). The two most significant flash address pins are connected to DSPA GPIO pins 9 and 10.

The flash device can be re-programmed by the DSP at any time. There is a software protection mechanism to stop most errant applications from destroying the device's contents.

The SMT395Q is fully supported by Sundance's SMT6001 flash programming utility.

2.2.2.3 External Memory

64Mbytes of SDRAM (2 x Micron MT48LC8M32B2, 8Mx32 each) is provided for each DSP. DSPA has an additional 64Mbytes of SDRAM.

256Mbytes of DDR memory (4 x Micron MT46V32M16, 32Mx16 each) is connected directly to the FPGA.

2.2.2.4 Virtex-II

This device, a Xilinx XC2VP70FF1704, is responsible for the provision of the two SHBs, comm-ports, global bus, the interface to the DDR memory, and RSL. On power-up, this device is un-configured (SRAM based FPGA technology). During the DSP boot process, the FPGA is configured for normal operation.

The standard configuration for the FPGA uses approximately 13% of the available logic. The remainder can be used for additional user functions.

This FPGA provides external comm-ports and 6 internal comm-ports which allow communication between the DSPs.

Each DSP has 4 comm-ports. One of these is external, and the other 3 are for inter-DSP communications.

2.2.2.4.1 Core Temperature Sensing

The FPGA's core temperature is monitored. If an over-temperature condition is detected (greater than 85°C), then the FPGA will be shut down and the done LED will illuminate. There is no method for informing the DSPs of this event, as all external interrupt pins are routed via the FPGA. What will happen is that all FPGA registers will read back as 0xFF. As soon as the temperature goes below the threshold, then the FPGA can be re-configured.

2.2.2.4.2 External Comm Ports

These communication links follow Texas Instrument C4x standard. They are 8-bit parallel inter-processor ports of the 'C4x processors.

The 395Q follows the C40 TIM standard with regard to the operation of these links. The diagram on the next page shows all internal and external comm ports.

A connection can only be established between comm-ports with a different reset state. On each TIM the links 0, 1 and 2 are set to transmit at reset and the links 3, 4 and 5 are set to receive at reset. Never connect two comm-ports of the same category together.

Always connect any one of comm-port 0, 1, 2 to any one of comm-port 3, 4, 5.

The transfer can start in any direction.

Additional information on the standard is available in the TMS320C4x User's Guide chapter 12: Communication ports and the Texas Instrument Module Specification.

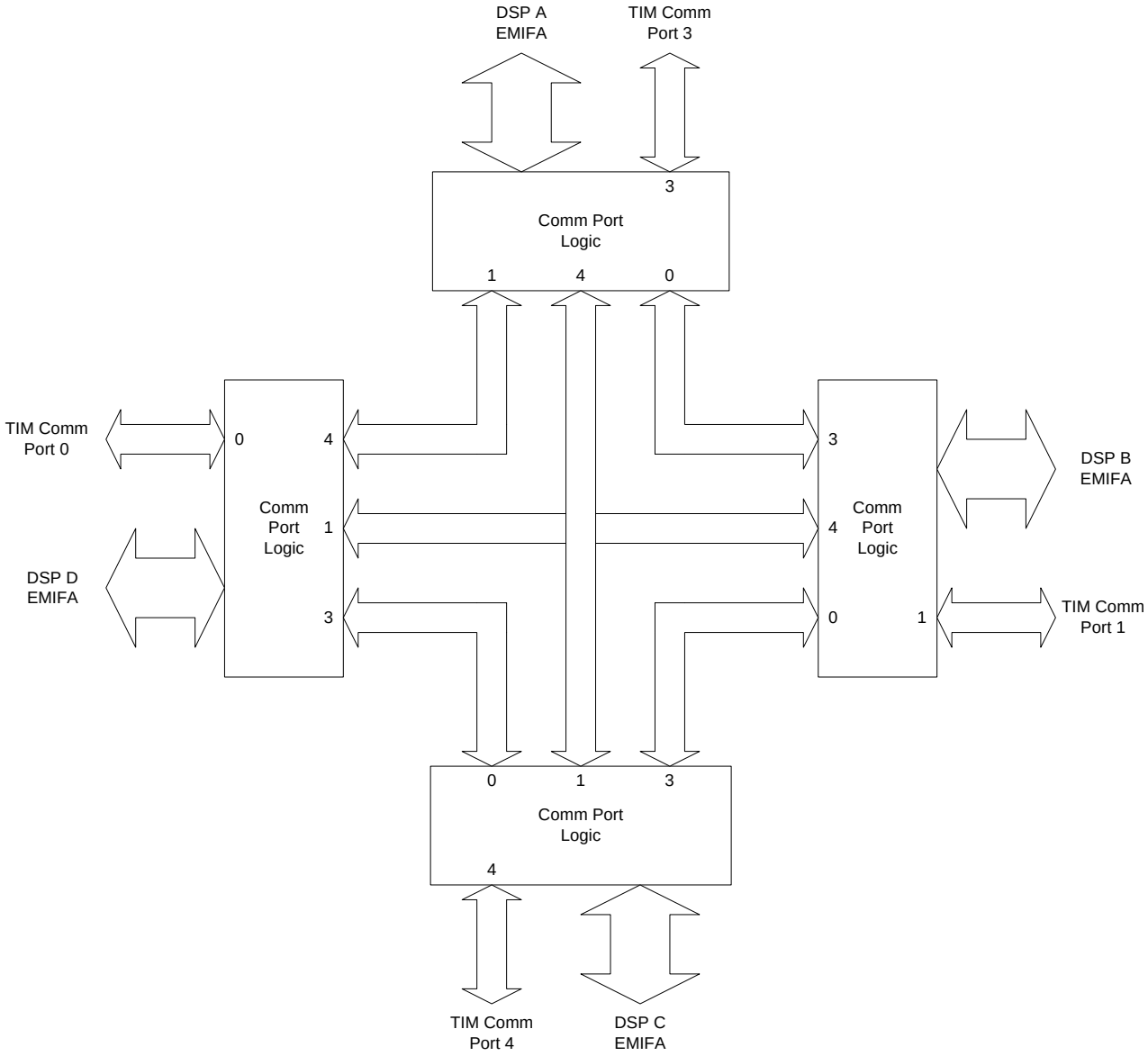
2.2.2.4.3 Internal Comm Ports

Each of the 4 DSPs (A, B, C & D) connects, via their EMIFA, to the FPGA. The FPGA implements 6 comm-ports which allow a fully interconnected topology.

In all respects, these internal comm-ports function (from a software point of view) identically to the external ones.

Each of the comm-ports (internal and external) is associated with two 16x32 bit unidirectional FIFOs (input and output) to be able to maintain a maximum bandwidth and to enable parallel transfer. They are guaranteed for a transfer rate of 20MB/s, which could lead, using the 4 comm-ports available to a 120MB/s external data transfer rate.

This diagram shows the external and internal comm-port connectivity.



2.2.2.4.4 External Clock

An external clock input is provided to the FPGA. This signal is directly connected to the secondary TIM connector user defined pin 12.

2.2.2.5 Serial Ports

Three serial ports are provided by the DSP. Two of these from each DSP are connected directly to the FPGA. The remaining McBSPs are interconnected between the DSPs to for a serial port 'ring'.

2.2.2.6 LEDs

Each DSP can control the state of 4 LEDs. These are connected directly to the GPIO pins 12..15.

There are an additional 4 LEDs which are controlled by the LED register within the FPGA, one per DSP.

2.2.2.7 Reset

Resetting the module will cause a hardware reset of all 4 DSPs and a re-configuration of the FPGA.

2.2.2.8 Booting

DSP A will boot from the code stored within the flash memory. This boot code will be responsible for configuring the FPGA, sending boot code to DSP B's HPI, and then loading applications via the first active ComPort, or from an application stored in flash.

DSP B will be responsible for booting DSP C, and DSP C for DSP D.

2.2.2.9 Power Supplies

This module must have 5V supplied through the TIM connectors. In addition, a 3.3V supply is required and should be supplied through the TIM mounting holes. This is compatible with the SMT310Q, SMT327 and future Sundance TIM carrier boards.

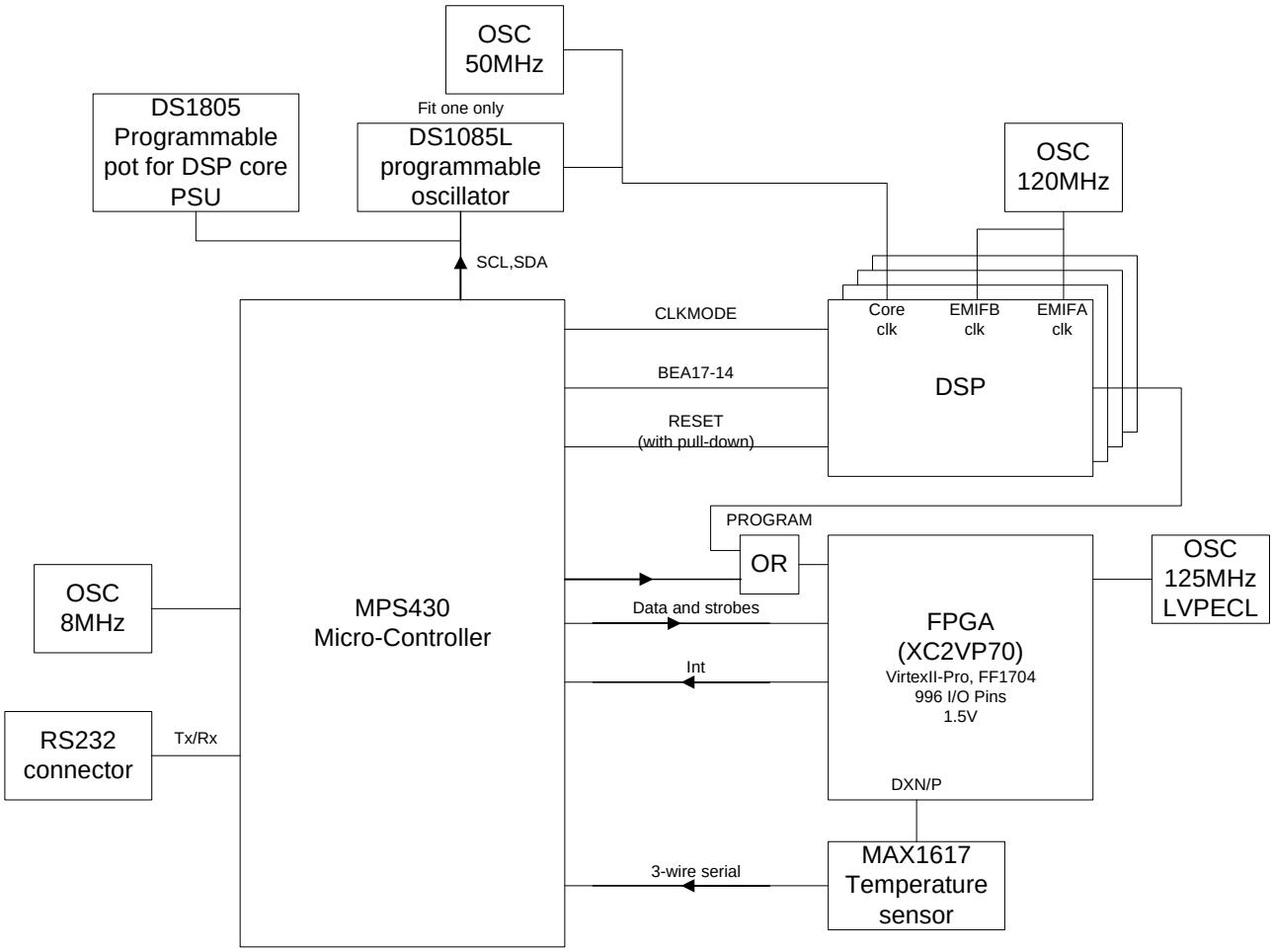
An additional power connection (standard floppy disk type) may be required depending on the FPGA configuration.

Contained on the module are DCDC converters for the DSP, DDR memory, and FPGA.

All supplies a guaranteed to meet the worst possible requirements of the FPGA.

2.2.2.10 System Control

Control of the system is provided via a TI MPS430 micro-controller. This is run at 8MHz, and provides several dozen user-defined pins. These are connected as shown below.



Starting at the top, the MPS430 is connected via an I^2C serial bus to a DS1805 programmable potentiometer. This pot is inserted into the DC-DC converter feedback, and thus can be used to adjust the DC-DC's output. The output is pre-set to 1.25V on power-up. The minimum value is 0.9V, and the maximum is above the Texas Instruments recommended voltage. Exceeding the absolute maximum voltage will cause damage to the DSPs.

Also connected to the I^2C bus is a DS1085L programmable oscillator. This enables a wide range of frequencies to be generated for the DSP core clock input. Alternatively, a fixed oscillator can be provided (build option).

The four DSPs share two oscillators for the EMIF bus speed. EMIFB is run at 50MHz, whereas EMIFA is run at 120MHz. The MPS430 is able to hold the DSPs in a reset state, and then it can change the CLKMODE (PLL multiplier), and EMIF bus speed options (via pins BEA17-14).

The assertion of the FPGA's PROGRAM pin (clears the configuration) is under control of both the MPS430 and the DSP (connected to BCE2). The MPS430 will assert this pin if it detects that the FPGA's core temperature has risen to an unacceptable level.

There is an 8-wire interface between the MPS430 and the FPGA. The signal functionality is shown here;

Signal	Function
F0	Data 0
F1	Data 1
F2	Data 2
F3	Data 3
F4	RD strobe
F5	WR strobe
F6	Reset
F7	Int

Data 0 to 3 form a 4 bit data bus. Data is sent from the MPS430 to the FPGA using this bus. The FPGA reads this data into a dual port FIFO. The FPGA can access the other port at any time.

The FIFO is written to on the rising edge of the WR strobe. The FIFO pointer increments on the falling edge.

The FPGA drives the data bus from a separate FIFO when it sees an active high on the RD strobe. The FIFO pointer is incremented on the falling edge of this strobe.

The WR and RD strobes are not active at the same time.

The reset signal (active high) is used to reset the RD and WR pointers in the FPGA.

When the FPGA has written new data for the MPS430 to read, it signals this fact be driving Int low. The FPGA will keep Int low until the MPS430 has read the last location of the FIFO.

Example VHDL code is given in files;

smt395q-test.vhd

ram_64x4.vhd

The FIFO data structure (MPS430 to FPGA) is shown here;

Location	Value
00-03	Gen. Purpose 1
04-07	Gen. Purpose 2
08-0B	DSPA 3.3V
0C-0F	DSPA core
10-13	DSPB 3.3V
14-17	DSPB core
18-1B	DSPC 3.3V
1C-1F	DSPC core
20-23	DSPD 3.3V
24-27	DSPD core
28-2B	DDR high
2C-2F	DDR low
30-33	FPGA high
34-37	FPGA low
38-3B	DSP core PSU
3C-3F	FPGA temp

DSPn 3.3V is a value that equates to the corresponding voltage using this equation;

V = (DSPn3.3V / 4096) * 3.3

DSPn core is a value that equates to the corresponding voltage using this equation;

V = (DSPn core / 4096) * 2.5

The DDR, FPGA, and DSP core PSU voltages are also referenced to a fraction of 2.5V.

i.e.

V = (value / 4096) * 2.5

The DSPn 3.3V supply is passed through a 0.150 Ohm resistor.

The DSPn core supply is passed through a 0.056 Ohm resistor.

Knowing the voltage drop across these resistors, the current (and hence the power) can be calculated.

The FIFO data structure (FPGA to MPS430) is shown here;

Location	Value (hex)
00-03	~Gen. Purpose 1
04-07	~Gen. Purpose 2
08-0B	Rsvd
0C-0F	Rsvd
10-13	OS
14-17	DAC
18-1B	MUX
1C-1F	Rsvd
20-23	Core vltg
24-27	~Core vltg
28-2B	Core PLL mult.
2C-2F	EMIFA speed
30-33	EMIFB speed
34-37	Rsvd
38-3B	Rsvd
3C-3F	Rsvd

The OS, DAC and MUX values are written directly into the DS1085L registers (programmable clock generator). Reference to the Maxim datasheet is recommended.

The Core vltg value is written directly into the DS1805E device (programmable pot controlling the DSP core voltage). A value of 126 (dec) will produce a core voltage of 1.2V. The power-on value provides a core voltage of 0.9V (until the micro-controller finishes its power-on sequence, when the voltage will be set to 1.25V). Values greater than 126 will produce a voltage in excess of the TI recommended absolute maximum, and should therefore be avoided. The ~Core vltg value is the complement of Core vltg. If ~Core vltg is not the complement of Core vltg, then no core voltage setting will take place.

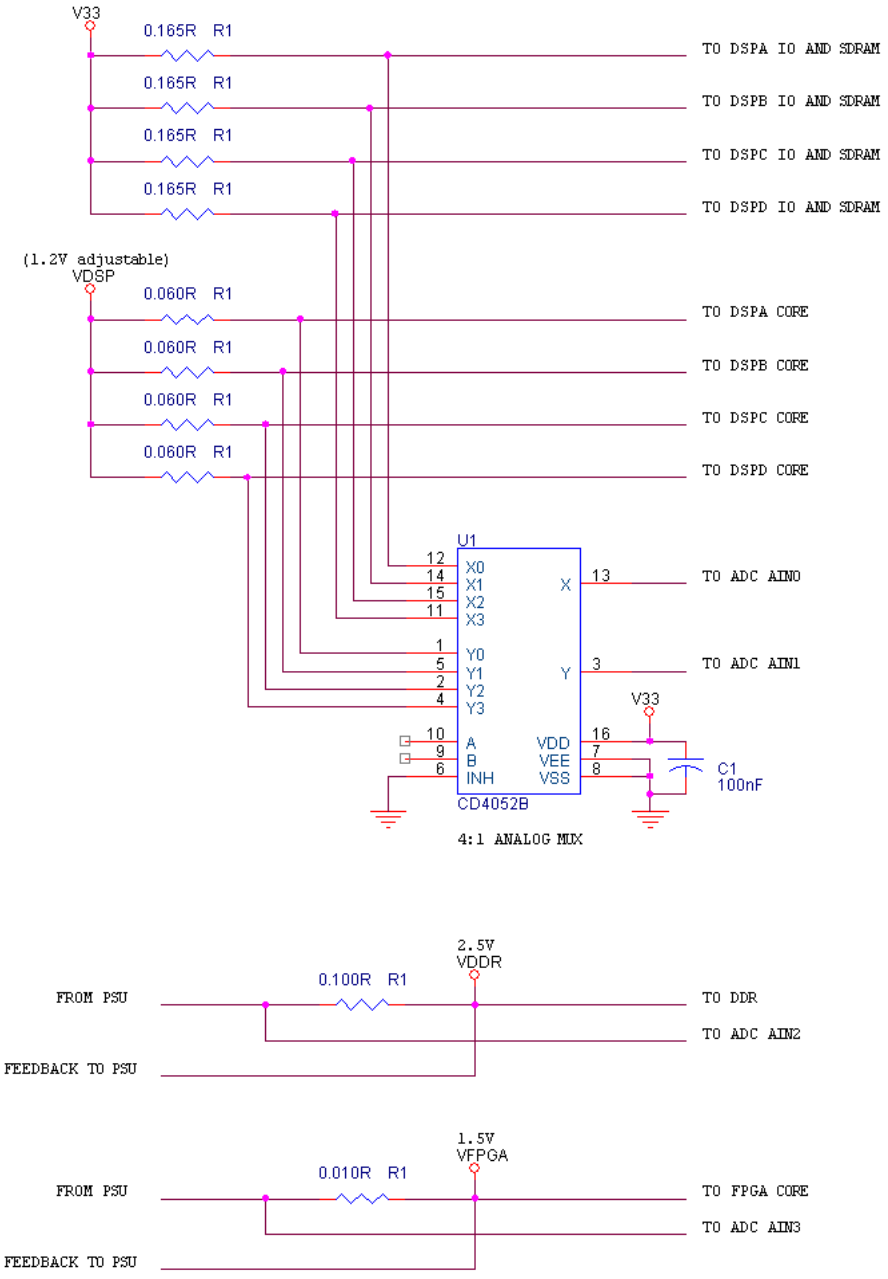
The maximum core voltage value is stored in non-volatile memory and cannot be erased.

The Gen. Purpose registers are read by the MPS430. When the MPS430 reads these registers, it checks to see if they contain the values 0x0055 and 0x00AA. The MPS430 uses this as a check to see if the FPGA has been configured and thus can determine the validity of the other read data.

A MAX1617 temperature sensor is connected to the MPS430 to enable it to monitor the FPGA's core temperature.

2.2.2.11 Power Measurement

Several of the major power supplies can be measured using an 8 channel ADC which is part of a micro-controller. The schematic is shown below.



Series resistors are fitted inline with the output of the power supplies (DSP core and SDRAM) to be measured. The value of these is chosen so that the voltage drop will not exceed 5% under maximum load.

The other two power supplies (DDR and FPGA core) have series resistors, but the output from the resistor is fed back to the power supply. This ensures that the device always receives the correct voltage. The voltage on the power supply side of the resistor will therefore be higher.

The ADC allows for several different voltage references (internal and external). It is a 12 bit converter, so can produce 4096 codes over the input voltage range Vref- to Vref+.

The table below shows the ADC parameters. '#' refers to the number of different ADC codes produced over the series resistor voltage drop range.

Device	Voltage	Current	Resistor voltage drop	Vref+	Vref-	#
SDRAM & DSP I/O	3.3	1.00	0.165 (5% of 3.3)	3.3	0	205
FPGA core	1.5	10.00	0.1*	2.5	0	164
DDR	2.5	1.00	0.1*	2.5	0	124
DSP core	1.2	1.00	0.060 (5% of 1.2)	2.5	0	164

*Voltage drop is set and then the resistor value calculated.

E.g. For FPGA, set voltage drop to 0.1V, then R = 0.1/10 = 10mOhms. Larger voltage drops may be possible which would increase #.

The micro-controller (MPS430F148) continuously monitors all parameters. All voltage measurements (and the FPGA core temperature) are via the 4-bit data bus to the FPGA.

A pre-set maximum FPGA core temperature is programmed into the micro-controller. If this temperature is exceeded, then the micro-controller will force the FPGA into an un-configured and non-operational state.

For greater power measurement accuracy, the voltages across the series resistors can be monitored using an external volt-meter.

Alternatively, the resistors could be removed and ammeters inserted for direct current measurement. It is suggested that this is NOT undertaken, as failure to ensure all power supplies are within tolerances (i.e. If an ammeter is not in circuit when power is applied), may result in device damage.

3 Diamond Issues

The SMT395Q is essentially the same as the SMT395. A new processor type SMT395_NOEX is therefore defined, and an SMT395Q configuration would look like:

```
PROCESSOR DSP1A SMT395
PROCESSOR DSP1B SMT395
PROCESSOR DSP1C SMT395
PROCESSOR DSP1D SMT395
WIRE ? DSP1A[1] DSP1B[4]
WIRE ? DSP1A[4] DSP1C[1]
WIRE ? DSP1A[0] DSP1D[3]
WIRE ? DSP1B[3] DSP1C[0]
WIRE ? DSP1B[4] DSP1D[1]
WIRE ? DSP1C[3] DSP1D[0]
```

4 Power Consumption

Approx 10.6W running standard firmware, DSPs idle, 1GHz core.

5 Verification Procedures

The specification (design requirements) will be tested using the following:

1) Running Code Composer
2) Running 3L Diamond
3) External interface tests (ComPort, SHB, Global Bus)and memory tests.

6 Review Procedures

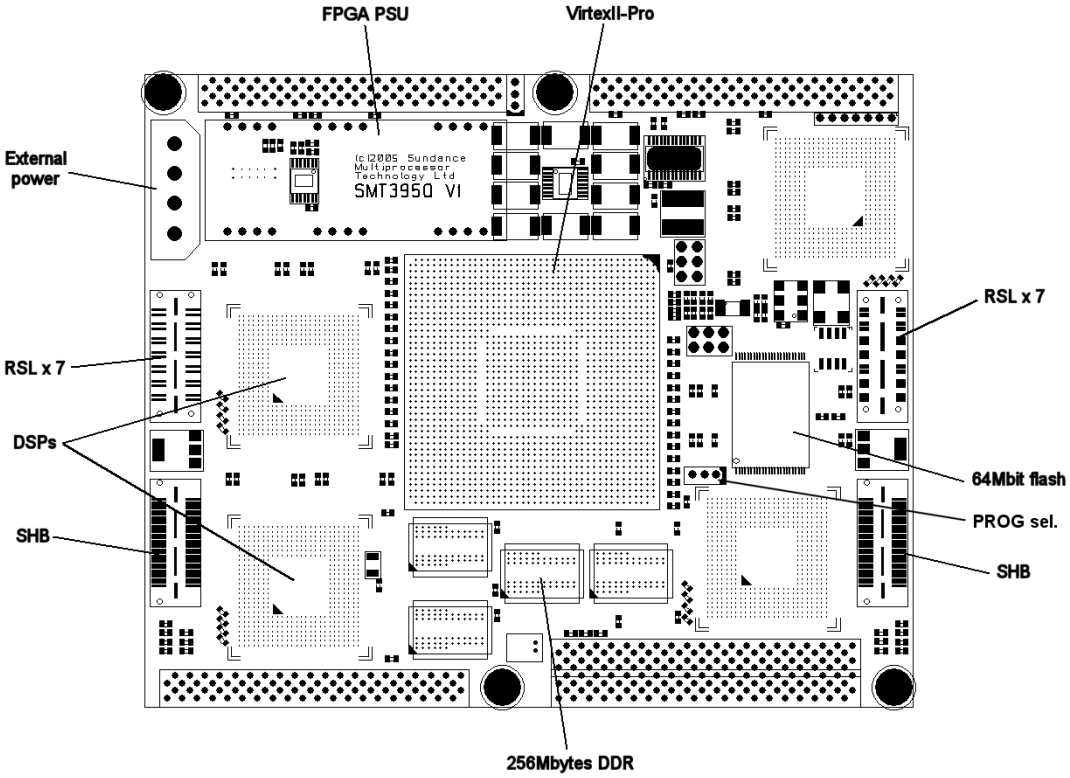
Reviews will be carried out as indicated in design quality document QCF14 and in accordance with Sundance's ISO9000 procedures.

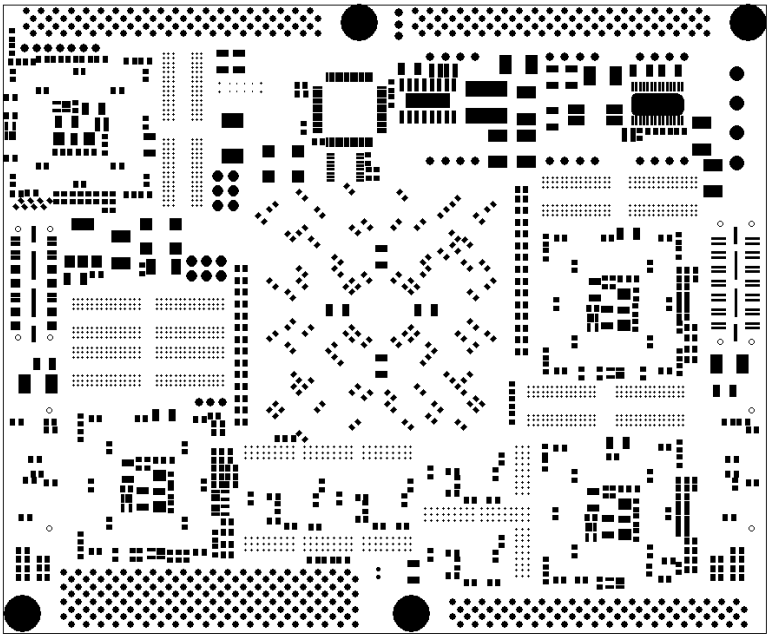
7 Validation Procedures

8 Circuit Diagrams

9 PCB Layout Details

9.1 Component Side





10 Pinout and Package Requirements

10.1 SHB pin-out

Pin			Signal	Pin			Signal	Pin			Signal
1			CLK0	21			D19	41			D39
2			D0	22			D20/ WEN1	42			D40
3			D1	23			D21/ REQ1	43			D41
4			D2	24			D22/ ACK1	44			D42
5			D3	25			D23/ CLK2	45			D43
6			D4	26			D24	46			D44/ WEN3
7			D5	27			D25	47			D45 REQ23
8			D6	28			D26	48			D46/ ACQ3
9			D7	29			D27	49			D47/ CLK3
10			D8/ WEN0	30			D28	50			D48
11			D9/ REQ0	31			D29	51			D49
12			D10/ ACK0	32			D30	52			D50
13			D11/CLK1	33			D31	53			D51
14			D12	34			D32/WEN2	54			D52
15			D13	35			D33/REQ2	55			D53
16			D14	36			D34/ ACK2	56			D54
17			D15	37			D35/ CLK3	57			D55
18			D16	38			D36	58			D56/ WEN4
19			D17	39			D37	59			D57/ REQ4
20			D18	40			D38	60			D58/ ACK4

32-bit Interface
16-bit interface

This standard is implemented using SAMTEC QSTRIP 0.50mm Hi-speed connectors.

To improve electrical performances, a ground plane is embedded in each QSTRIP connector.

For long distances micro-coax ribbon cable is used to connect 2 QSTRIP connectors .

An SHB interface can be 8,16 or 32-bit wide.

11 Jumpers/Links

11.1 JP3 – Prog Sel.

The position of this jumper determines the way the FPGA's PROG pin is controlled.

With the jumper to the right (towards pin 1, factory default), the PROG pin can be asserted by either DSPA or the micro-controller (over temperature condition).

With the jumper to the left, the PROG pin will be asserted low continuously. This can be useful if a non-functioning bitstream has been loaded which could potentially prevent re-programming of either the FPGA or flash memory.

With the jumper removed, the PROG pin cannot be asserted, and thus the FPGA can be configured only once (until power cycled). This is strongly advised against as the over-temperature control is also bypassed.

[Note that future versions of this module will allow the over-temperature condition to assert PROG regardless of the jumper setting]

11.2 JP1 – FPGA JTAG

This table shows the pin-out and organisation of the FPGA's JTAG header.

Signal	Pin	Pin	Signal
GND	6	3	TCK
TDO	5	2	TMS
TDI	4	1	Vcc

Connect this header to a Xilinx Parallel Cable IV, for directly loading custom bitstreams.

11.3 JP2- TTL I/O

This table shows the pin-out and organisation of the TTL I/O header.

Signal	Pin	Pin	Signal
GND	6	3	TTL1
TTL3	5	2	TTL0
TTL2	4	1	3.3V

These signals are unused within the standard Sundance FPGA firmware. They are directly connected to the FPGA and can be used as either input or output of LVTTL (3.3V) signals. Useful for test/probe points.

12 Safety

This module presents no hazard to the user.

13 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.