Ultra-wideband Multichannel Receiver Test Bed

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***Abstract*— Developing a test bed for the study of UWB (Ultra Wide Band) MIMO (Multi Input Multi Output) systems requires unique capability not necessarily found in common commercially available devices. Some of the characteristics attractive to research test beds are impractical when applied to commercial solutions, this is especially true of UWB where commercial devices targeting accepted applications and changing government standards dictate fairly narrow confines for the operation of UWB signals. This paper is an overview of the techniques, challenges and solutions adapted to a custom receiver front end allowing minimum distortion, noise and interferences while providing the researcher with the most adaptable platform we could provide for the research being performed on the Tennessee Technological University UWB MIMO test bed. In addition, phase noise in the distributive clock is discussed as well. Finally, we introduce the digital section built on a customized multichannel digitizer that is capable of processing data in real time.**

***Index Terms*— MIMO, UWB, Low Noise Design.**

I. Introduction

The verification of new concepts and theories regarding identification of signal sources and spectra in UWB requires a pristine test environment. Many commercially available software defined radio (SDR) test beds and components are however designed for specific established markets. In order to achieve the highest quality platform while maintaining spectrum flexibility, it became necessary to look into customizing the design of the UWB MIMO test bed using available technologies, while leveraging the building blocks common to such systems. Ideally the researcher would hope to find that the test system would have as little impact or limitations on verifying the theory with empirical measurements as possible. The design approach the research team has taken is to build a semi-custom test bed that has very large bandwidth, channel flexibility and a modular design capable of morphing into several form factors useful in exploring new concepts. Such a "wish-list" design is still not entirely practical, but with proper management many of the goals can be achieved. The ultimate goal is for the MIMO test bed is to perform its functions with as little impact on the raw signals as possible prior to data translation and processing. This concept depends on using techniques that are typically impractical when viewed from a complexity / practicality standpoint with an eye towards reliability and manufacturability. The goal is however to build a one-off test bed for use in UWB research so such impracticalities are considered secondary to the design purpose. It is for this reason the design team has chosen to forego the lure of commercially available SDR test platforms and design a modular test bed specifically for our use.

The rest of this paper is organized as follows. Next section presents an engineering design of low noise amplifier (LNA) with ultra wide bandwidth, large variable gain range and very low noise figure. Initial measurement results of the implemented LNA are reported in section III. In section IV phase noise issue associated with the clock circuitry is addressed. Section V introduces the design and implementation of the digital section based on a wideband digitizer with certain real-time processing capability, followed by section VI to conclude the paper.

II. Low Noise Amplifier (LNA)

A. Design Criteria

The first step was to define the receiver front end, ideally in UWB we want low noise figure(NF) with very high bandwidth. DC - 5.0 GHz and reasonable gain 15db - 80 db. Practically we can come very close, especially when leveraging some of the newer SiGe LNA devices available. The low NF typically less than 1.0 db coupled with bandwidths as high as 4 GHz make these devices desirable. The design will sacrifice NF in the subsequent gain attenuation stages, however layout and power supply design will prove more important and allow us to mitigate some of these performance losses. It has been suggested that variations in the oscillators and particularly the phase lock loops, (PLL) circuits that phase noise in such circuits can be attributed to fluctuations in the power supply [1] [2]. Indeed ideally, aside from the Additive Gaussian White Noise (AGWN) the flicker noise or electron recombination makes up the bulk of the noise found in LNA amplifiers. These noise sources are inherent to the physical properties of the amplifier itself, and practically this is the noise presented when a manufacturer discusses the NF and noise characteristics of the amplifier. However this is value tested under ideal situations where the fluctuations of the DC power supply are minimal if not near non-existent. Additionally in the case of multiple channel MIMO receivers the distribution of local oscillators and reference clocks is equally of concern. A carefully measured phase difference between two or more matched receivers can allow the researcher to adapt and correct for these anomalies and help restore the data sets to their ideal. The design concerns itself with reducing these fluctuations

as much as possible to help make this calibration task easier and less setup dependent. The impact of the clock distribution and recovery will be explored as a prerequisite for any design choices made.

B. Practical approach

Having established the design criteria for the UWB MIMO receiver front end, we must make decisions in order to come as close as possible to our design goals. The receiver amplifier has the following characteristics.

- Gain – 15db - 80db user adjustable.
- Noise Figure $<$ 3db.
- Wide Bandwidth – 10 MHz - 3000MHz.

The amplifier incorporates an extremely low noise regulator with a voltage follower bandwidth of 900MHz, this reduces the noise floor of the supply acting as both a regulator and a large bandwidth filter on the supply rails. Measured ripple on the 5Vdc supply pins has been measured a ¡ 50uV rms. Additionally all digital control interfaces to the variable attenuators are optically coupled with filtered single bridges to a common ground point [3]. This low noise approach reduces the LNA noise to the intrinsic flicker, Johnson recombination noise, and to the AGWN expected in such wideband high gain configurations. Any induced phase noise not present in the recived signal is reduced by eliminating the current paths associated with this additive source. The RF PCB is designed using Rodgers 5880 material and a hard gold flash finish on all exposed traces. The center target frequency of 850 MHz within our 200Mhz - 1.5GHz design goal is the basis for the dimensions of the ground coplanar wave guide, modeled using AWR corporations Microwave office. The LNA uses a 15db gain wideband amplifier from RF Micro devices, which is cascaded into dual 0 - 31db digitally controlled amplifier/ attenuators. This gain control gives the researcher a high degree of flexibility when modeling the sensitivity of an individual MIMO channel.

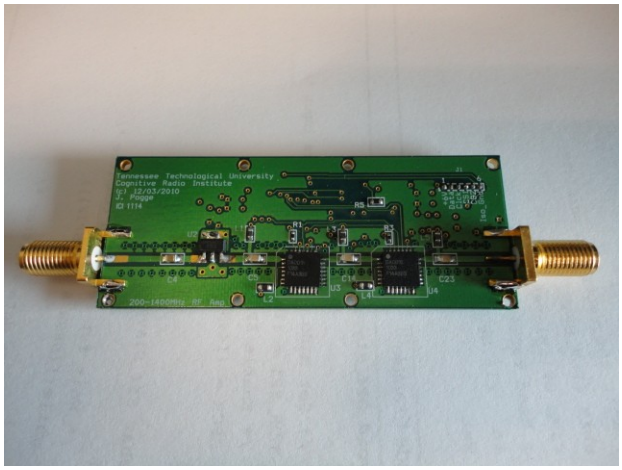

Fig. 1. MIMO Receiver Amplifier.

III. INITIAL RESULTS

A series of LNA front end prototypes were built using the above design specifications, currently revision (A). The LNA resides on an independent circuit board such that configuration of any number of MIMO receiver channels can be experimented with by adding additional channels. Power supplies and control interface are filtered and isolated from the RF circuitry such that very little system noise can migrate into the signal under test. Once a desired gain has been set the control interface can be completely powered down to eliminate any additional noise current paths. The goal here is to provide receiver LNA capability over a wide band with large dynamic range and as little phase and signal distortion as possible.

A. Transmission Charcteristics (S21)

The amplifier was set for a gain of 25db and characterized on an Agilent model 8753ES network analyzer, The analyzer is limited to 3 GHz full scale, as expected there is some drop in overall gain as the frequency increases. The gain ranges from 28db at 10 MHz and drops to 18db at fullscale 3GHz. As shown in Fig. 2 the LNA performs well across the entire band.

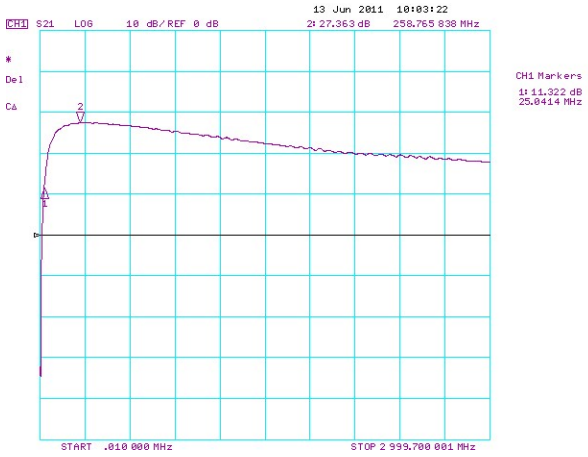

Fig. 2. DC - 3GHz Transmission Characteristics.

B. Phase Response

The device under test is essentially an inverting amplifier and as such has an inherent phase shift. The concern to the researcher is that the LNA adds any unwanted phase delay to the measured results. In particular we are interested that the phase of the LNA is flat throughout the desired band. In this design we are looking at 200MHz - 1.5Ghz as specified, however this LNA is capable of 100KHz - 3GHz with relatively good phase stability over the desired band. Fig. 3 shows an electrical delay of approximately 3pS throughout the desired band.

The twin cascaded Attenuator Amplifiers allow adjustment of the LNA gain between 15db and 78db in 0.5db steps, controlled via a test microcontroller board. This gain control can also be set via a standards serial peripheral interface (SPI)

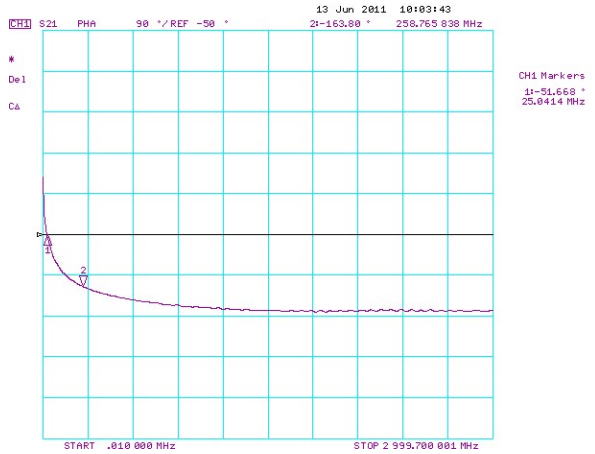

Fig. 3. DC - 3GHz LNA Phase Plot.

port on the test bed FPGA. All regulation and control signals are isolated to the back of the PCB separated by the ground layer and optically isolated control signals, as shown in Fig. 4.

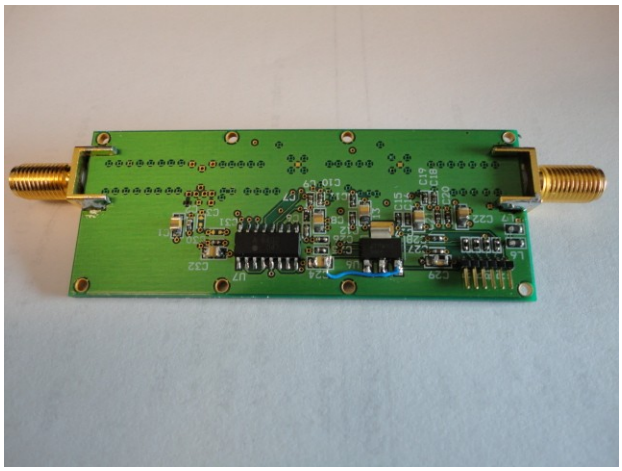

Fig. 4. DC regulators and optical isolation is located on the back of the circuit.

IV. PHASE NOISE IN THE DISTRIBUTIVE CLOCK

The UBW MIMO test bed can consist of two or more individual receiver channels and as such a concern is that the distributed reference clock used in down converters and ADC clock signals can be distorted by the clock distribution scheme [4] [5] [6]. An advantage has been seen in using a relatively low frequency reference clock and providing necessary frequencies for the local oscillator(LO) analog to digital conversion (ADC) clocks at the point of use. This test bed will use a distributed low frequency clock reference using isolated differential distribution techniques. All up/ down conversion or high frequency PLL, ADC conversion clocks as well as sources for the FPGA will be generated at the point of interest using this distributed clock. The intended master clock must have the following attributes to meet our design needs.

- Out of band- 10 MHz or less.
- Sine wave – to eliminate harmonics.
- Easily interfaced as a synch signal to available test equipment. (10 MHz looks to be a unofficial standard).

Low phase noise fractional-N synthesizers will use this common reference at the point ofservice, as this allows the design team to keep the high frequency traces isolated and short [1] [7]. Although commercially impractical, all oscillators will be located directly where needed rather than bussed or distributed from a single source Slight variations can be controlled through software calibration techniques or handled individually. Phase distortions due to varying lengths of the reference 10 MHz are either non-existent or easily managed in software [1]. System control can monitor the frequency and lock of any of the clock PLL circuits thus making troubleshooting of error signals much faster. The overall test bed is more flexible due to fact unused reference channels can be powered down without effecting the load or stability of any of the other MIMO channels.

A. Phase Noise Model

Phase noise in the received signal is additive [1]. The received I and Q modulated signal $r(t)$ with phase noise $\varphi_n(t)$, is given as:

$$r(t) = (i(t) + x(t)) * \cos(\omega(t) + \varphi_n(t)) - (q(t) + y(t)) * \sin(\omega(t) + \varphi_n(t)) \quad (1)$$

where $i(t)$, $q(t)$ are the received modulation signals, $\omega(t)$ is the carrier and $x(t)$, $y(t)$ are the thermal noise components, i.e., (AWGN) [1].

The reduction of external noise sources should bring our LNA very close to the modeled prediction. In this case we isolate the noise current paths through the power supplies and filter the reference signal through the use of properly chosen bypass capacitors [3]. Using a laboratory RF source of -40db signal at 850 MHz (center band) a phase noise measurement was taken using the Agilent 4440A Spectrum analyzer. The resulting plot show a very reasonable phase noise response by the LNA. The phase noise was measured at both extremes of the UWB LNA, 200MHz and 2.0 GHz, with a gain setting of 25db, and an RF source signal of 25db. Fig. 5 shows the 200 MHz phase noise measurement with all signals above 10 KHz around -100dbc/Hz .

The same measurement was taken highest design frequency of 2 GHz, Fig. 6 at an amplitude of -25dbm, with a gain of 25dbm. Here we see a slight improvement at the same point of 10KHz, the gain degradation coincides linearly with the reduction of phase noise level of -105dbc/Hz vs the previous -100dbc/Hz with the 200MHz carrier. The gain was reduced by 5dbm as is expected from the measurement seen in Fig. 1.

V. MULTI-CHANNEL GHZ DIGITIZER WITH FPGA ARRAY

Besides the multi-channel wideband RF front-end, a complete solution for a multi-channel GHz digitizer with FPGA array is also considered in the authours' laboratory. Thanks to recent advances in semiconductor technologies, commercially

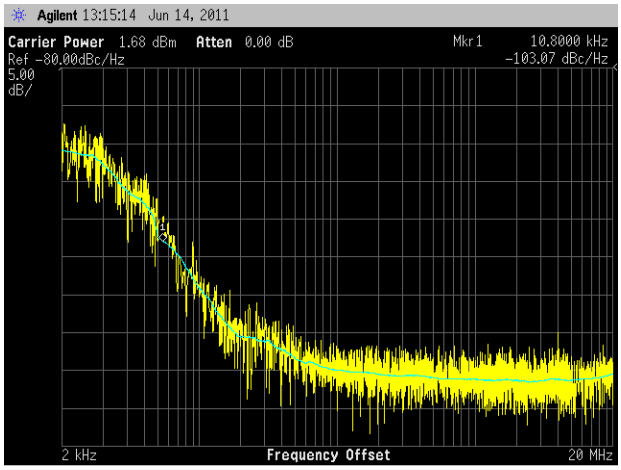

Fig. 5. 200 MHz -25db Phase Noise Measurement.

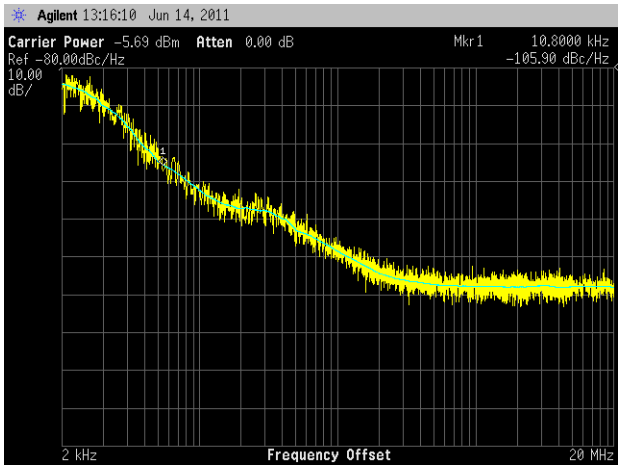

Fig. 6. Phase Noise measurement at 2 GHz -25dbm Input.

available Field-programmable Gate Array (FPGAs) provide more and more processing power and increasingly support faster inter-device digital interfaces. This trend makes it feasible to perform wideband multi-channel processing within the digital domain. Such capability enables exploration of various advanced wideband MIMO and wideband cognitive radio algorithms on flexible FPGA firmware-based platforms.

A. Products Selection Criteria

For a wideband multi-channel system with 500 MHz bandwidth, the Aanalog-to-Digital Converter (ADC) needs to have a least a sampling rate of 1 Giga-Samples Per Second (Gsps), in practical applications 2 Gsps is desirable. Further more, large dynamic range and sampling of wideband signals demand high precision ADCs. There is however a fundamental tradeoff in ADC resolution vs, sampling speed. The requirement of a multi-GHz speed ADC necessitates the dynamic range of the signal be reduced before conversion.

Additionally a powerful data buffer is necessary to organize and store such large high speed data streams, the best choice is to locate the buffer and the ADCs on a single board. The digital portion should be capable of receiving the digital samples as well as handle the necessary processing at a high speed. This realization suggests the connection between the sampling and buffer section will be a problem. On the other hand, the processing capability and intrinsic overhead associated with processing is of concern. One obvious solution is to build a powerful FPGA array. The FPGA is a good candidate for implementing intense computations and complex systems due to its inherently fast parallel processing capability and relatively short design time. It becomes obvious, however, that any achievable FPGA performance is limited by the scale and distribution of the devices logic cells. If the number and arrangement of logic cells and arrangement of resources of one FPGA cannot fulfill the application, then an FPGA array solution is to be considered. The combining of several FPGA devices together in order to expand the number of processing paths and cell depth becomes an enticing option. When using FPGA arrays, however, there are some design challenges such as power consumption, synchronization and routing, which are much easier to handle in single device solution. Therefore the design of a distributive FPGA array must be very careful regarded when weighed against the overall system complexity.

Major selection criteria are summarized as below.

The ADC board has to meet the following criteria.

(1) The sampling rate can be up to 3 Gsps.
(2) There should be 2 sampling channels working at the same time within one board.
(3) There should be sufficient data buffers and storages embedded on the board.
(4) High speed connectors capable of handling the data and frequency required by the digital processing modules or PCs.
(5) Multiple boards should be able to work together and be properly synchronized

The FPGA array also has to meet the following criteria.

(1) The FPGA device should have sufficient processing capability for more than two channels.
(2) The FPGA board should have high speed connectors for interfacing with the A/D converter boards.
(3) The FPGA can be easily connected with each other to form an array and properly synchronized.

B. Hardware

Fig. 7 shows the hardware architecture of the implemented UWB multi-channel GHz digitizer with FPGA Array, there are totally eight ADCs each with 3 Gsps sampling and 8-bits resolution, an array of Xilinx high performance FPGA for digital processing and a bunch of 1GByte Double Data Rate 2 (DDR2) memory banks for data storage and buffering. All these devices are integrated in a NI PXIe hybrid chassis. All the ADCs sampled data will be gathered in one FPGA either to be processed in real-time or to be stored in DDR2 memories and then transfered to host computer via PXIe bus for offline processing. This system also has potential to be attached to a general-purpose computing on graphics processing unit (GPGPU) for more intensive computing.

To maintain the coherency of the MIMO receiver system, it is essential that all modules receive the same sampling

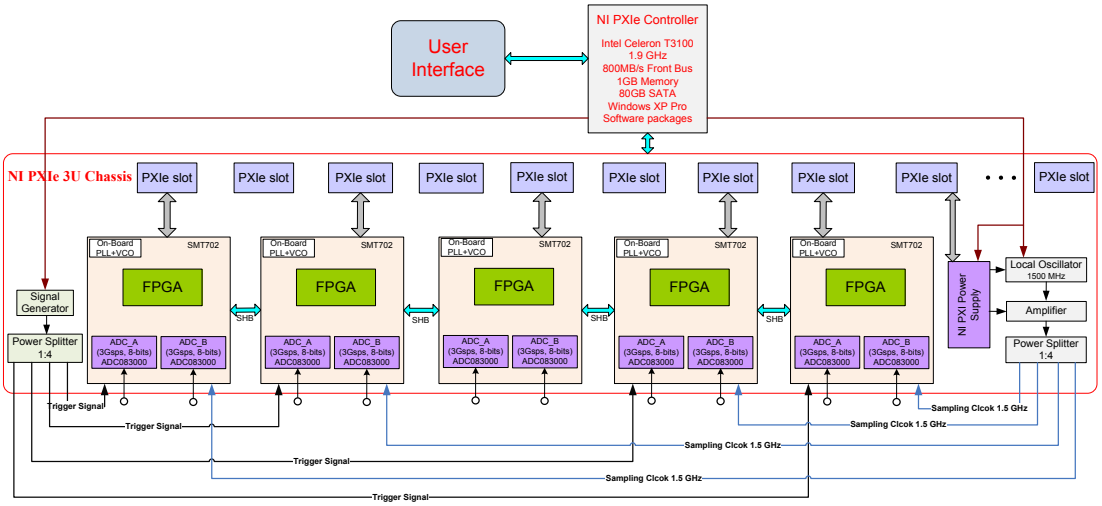

Fig. 7. Block diagram of the receiver's digital hardware hosted in a PXIe chassis

clock. In our case, there will be a single clock source that is distributed to the modules via a power splitter, thus all eight ADCs receive an identical clock in frequency and phase. Another design requirement of this system is to have all ADCs sampling and outputting data at the same time, so an external trigger is necessary to synchronize the converters and be part of the logic to reset the converters [8].

C. A Software Design Example

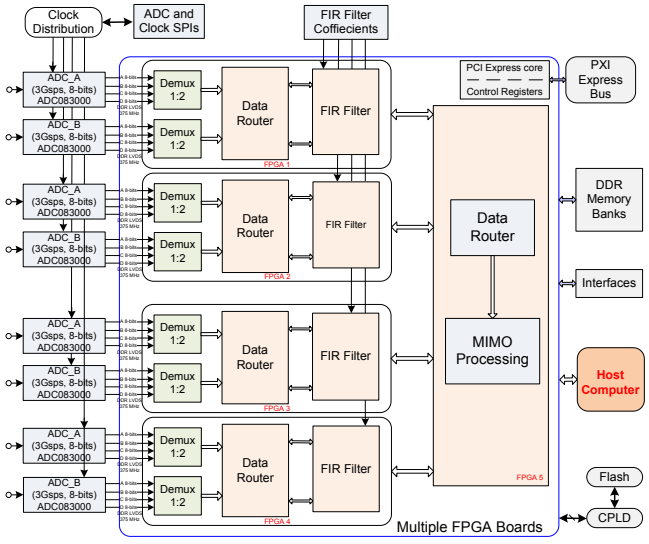

Fig. 8. Software design architecture of wideband digital beam forming

Fig. 8 is a software design example aiming at wideband digital beam forming, where there are 4 receive channels each with in-phase (I) and quadrature-phase (Q) components. The FIR filtering are applied to the sampled data of each channel, and all the filtered data can be combined in one FPGA device to form the final waveform. After the system is powered on, the ADCs and the clock generators will be configured to ensure they are all locked to a reference signal. At this point the sample stream from the ADCs will begin to be captured and stored. Inside the FPGAs, one digital clock manager (DCM) per ADC clock is used to ensure a good capture of the data. Once samples are clock in they are routed through multiplexers to be pipelined and latched again. Then various digital signal processing tasks can be applied to the each ADC sampled word. An alternative method is to store the samples into the DDR2 memory banks available on each board. The DDR2 interface uses some Xilinx specific blocks, such as Idelays and DCMs, which have to be 'locked' and 'ready' as well. Each ADC is dedicated to a DDR2 memory bank, which appears to the designer as a First-In First-Out (FIFO) buffer. These FIFOs have status bits used to check whether they are empty or full, and each FIFO is connected through a Direct Memory Access (DMA) channel.

The operation of one FIR filter function for each receive channel is given in Fig. 9, where parallel processing are largely used to relax the high sampling rate pressure for wideband signals. Assuming the sampling rate of input signals is 1 Gsps, the serial to parallel converter rate and serial to parallel converter can be set as 1:8 and 8:1 respectively, thus the basic processing is only 125 MHz, which does not put too much burden to FPGA devices. Diagram of the operation of each FIR filter is shown in Fig. 10. The delays result from operating on prior input samples, and f_s is the sampling frequency (after 1:8 serial to parallel converter, f_s is 8 times of the input signal before the conversion). The C_n values are the filter coefficients used for multiplication and it has both I and Q parts, so that the output at time n is the summation of all the delayed samples multiplied by the appropriate coefficients. The filter then inputs another sample of data (which causes the oldest sample to be thrown away) and repeats the process. The process of selecting the filter's length and coefficients is critical in the filter design. The goal is to set those parameters such that certain desired signals are strengthened and others are attenuated.

In our preliminary FIR filter design, we consider 64 taps each with 8-bits width and each tap consists of both I and Q parts. The input data width is preset as 8-bit; the output data width of each FIR core is 24-bit; the final output data width for

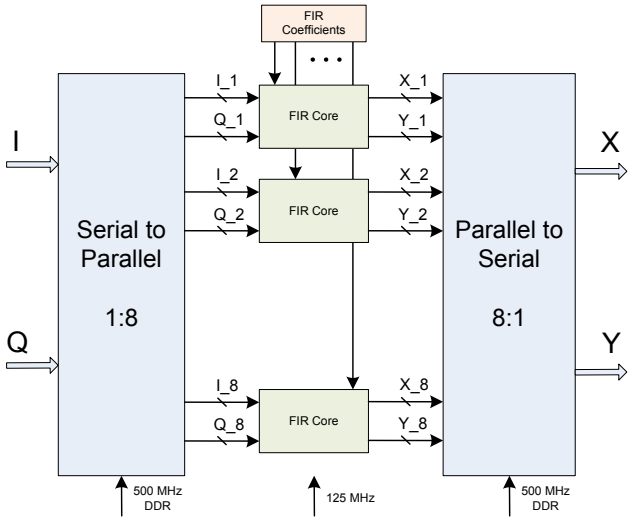

Fig. 9. Structure of one FIR filter for each receive channel with both I and Q components

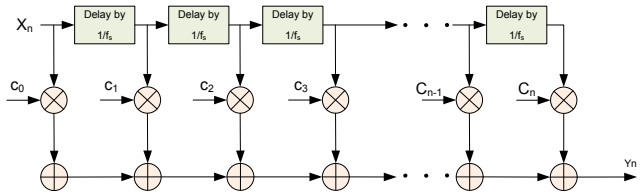

Fig. 10. Structure of FIR filter core

each receive channel is 25-bit, which are rounded to 8-bit in current design and could be easily expanded. The design has been implemented in Xilinx Virtex-5 FX70T FPGA, and the resources usage statistics are given in Table I. As we can see, the multiplication computations, represented by DSP48Es, are tremendous heavy and account for a substantial percentage of the total resources usage.

TABLE I
FIR FILTER FPGA IMPLEMENTATION STATISTICS FOR ONE RECEIVE CHANNEL

FIR filter	Amount used	Percent used
Number of Slice Registers	108	1%
Number of Slice LUTs	48	1%
Number of occupied Slices	39	1%
Number of bonded IOBs	19	2%
Number of BUFG/BUFGCTRLs	3	9%
Number of OSERDESs	32	NA
Number of PLL_ADVs	1	16%
Number of DSP48Es	126	98%
Total equivalent gate count	1,472	NA

VI. CONCLUSION

This paper presents a portfolio of designs with emphasis on the RF front end and digital back end in the UWB multichannel receiver test bed. Some design tricks, test results and hardware configurations are provided. The developed test bed can serve as a general UWB experimental research platform, and it can be easily extended to emulate a wideband beamformer or conduct certain MIMO radar experiments. This receiver test bed will continue to evolve in order to support our ever-growing research. What can be anticipated in the near future include: 1) frequency-agility in the front end; 2) low phase noise, flexible and scalable clock distribution for distributed receiving sensing nodes; 3) ability to save processed data automatically; and 4) high-speed data connection between the digitizer and an off-board PC.

VII. ACKNOWLEDGMENT

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