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VF360

Stratix® V FPGA module with DSP and FMC for demanding computation and I/O applications

OpenVPX
FMC™

SPECIFICATIONS

Processing FPGA

- Stratix V family in the KF40 (1517 FBGA) package
  - GX Device variants: 5SGXA3, 5SGXA4, 5SGXA5, 5SGXA7, 5SGXA9 and 5SGXAB
  - GS Device variants: 5SGSD4, 5SGSD5, 5SGSD6 and 5SGSD8
- Embedded device memory: 19-52 Mb
- Embedded device multipliers (18x18): 512 – 3,926
- DDR3 and QDRII+ external memory
  - Up to 2GB DDR3 @ 667MHz (arranged as two 256M x 32-bit banks), default 1GB
  - Up to 32MB QDRII+ SRAM @ 400MHz (arranged as two 8M x 18-bit banks), default 16MB

Digital Signal Processor

- Ti KeyStone Multicore C667x family of processors
  - Up to 8 cores @ 1.2 GHz
- External memory: Up to 2 GB DDR3 @ 667MHz (matched to FPGA DDR3 size), default 1GB

FPGA Mezzanine Card (FMC)

- 10x High-Speed Serial Interface lanes
- LVDS interface on LA and HA

VPX Interface

- Comply with OpenVPX MOD3-PAY-3F2U-16.2.12-2 module profile
  - PCIe Gen2 Data plane (3x Fat Pipes)
  - GigE 1000BASE-BX Control plane (2x Ultra-Thin Pipes
  - Payload module with System Controller capability
- Supports FPGA configurable User I/O on P2
  - 24x single-ended 2.5V LVCMOS I/Os
  - 10x High-Speed Serial Interface lanes

Software and Firmware Support

- Board support package
- Linux and Windows PCIe drivers
- Sample application
- FPGA Firmware
  - reference design
- VR300 Test RTM with USB-Blaster II, XDS100 and Ethernet (via SFP)

FMC Companion Modules

- FM500 Test FMC with USB-Blaster II, XDS100 and mini-SAS interfaces
- FM550 Two Channel mini-SAS I/O FMC
- FM570 Dual Channel DAC FMC
- FM580 Eight Channel ADC FMC

The **VF360** is a 3U OpenVPX module that leverages on Intel Stratix® V FPGA and Texas Instruments KeyStone Multicore DSP technology to provide an ultra-high bandwidth processing platform, ideally suited for computation and bandwidth intensive applications such as Radar, Networking, SIGINT, EW, SDR and Video.

The onboard multicore DSP from Texas Instruments provides the flexibility to perform complex post processing functions more suited for the processor domain. High bandwidth communication between the DSP and FPGA is provided through both PCIe and Serial Rapid IO (SRIO) interfaces.

The Stratix® V FPGA has two banks of dedicated DDR3 and QDRII+ memories for algorithms with high bandwidth and/or large memory size requirements. High- speed serial interfaces to the OpenVPX data plane and the FMC site creates abundant FPGA IO throughput.

The **VF360** acts as an FMC carrier to provide a modular solution that accommodates a wide range of I/O requirements.

The **VF360** conforms to the OpenVPX standard and operates as a Payload module with System Controller capability. Both air-cooled and conduction cooled versions are available. Further flexibility is provided through build options to cater for 10 different FPGAs from Intel's Stratix® V GX and GS device families.

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SPECIFICATIONS

Typical Applications

- Radar Signal Processor (Doppler filter, Pulse compression, CFAR)
- Spectrum analysis in EW (Signal detection & classification, jammer control)
- Video and image processing (DCT, 1D/2D convolution, etc.)
- Software Defined Radio (SDR)
- Real-time DSP functions (DDC, FFT, FIR, NCO, etc.)

Ordering Information

Generic order code = VF360-A-B-C-D-E-F-G

- A: FPGA (A3, A4, A5, A7, A9, AB) for 5SGXA3, 5SGXA4, 5SGXA5, 5SGXA7, 5SGXA9 and 5SGXAB (D4, D5, D6, D8) for 5SGSD4, 5SGSD5, 5SGSD6 and 5SGSD8
- B: Speed grade (2 or 3) for Transceiver speed, (C or I) for Commercial/Industrial temp (1 to 4) for FPGA speed
- C: DSP (1, 2, 4 or 8) for TMS320C667X one, two, four or eight core
- D: DDR3 (2 or 4) GB total DDR3 memory (1GB | 2GB for FPGA + 1GB | 2GB for DSP)
- E: QDRII+ (16 or 32) MB total QDRII+ memory (two banks of 8MB | 16MB for FPGA)
- F: THERMAL (0 or 1) for air-cooled or conduction cooled
- G: Conformal Coating (0 or 1) for un-coated or coated

Standard order code = VF360-A3-3I4-4-2-16-0-0

- 5SGXA3 FPGA 3 | 4 speed grade (Industrial temperature)
- TMS320C6674 four core DSP
- DDR3 = 2GB, 1GB for FPGA (2x 512MB) + 1GB for DSP
- QDRII+ = 16MB (2x 8MB) for FPGA
- Air-cooled, un-coated

Contact factory for other order options

Block Diagram